What is claimed is:

1. A method of testing a plurality of memory circuits included in a semiconductor device, comprising steps of:

selecting the plurality of memory circuits and causing the memory circuits to perform a read/write operation;

comparing plural pieces of read data read from the plurality of memory circuits in a read operation with one another; and

comparing one of the plural pieces of read data with write data.

2. The method according to claim 1, wherein the step of comparing one of the plural pieces of read data with the write data includes comparing a specific one of the plural pieces of read data with the write data.

3. The method according to claim 1, further comprising a step of temporarily holding results of comparing the plural pieces of read data with one another.

4. The method according to claim 1, further comprising a step of temporarily holding the plural pieces of read data.

5. The method according to claim 4, further comprising a step of temporarily holding results of comparing the plural pieces of read data with one another.

6. A semiconductor device comprising:

a plurality of memory circuits each of which performs data writing and data reading;

a processing unit coupled to the plurality of memory circuits for accessing one of the plurality of memory

circuits for data writing and data reading by supplying an address signal thereto;

an address decoder coupled to the processing unit for receiving the address signal and generating a plurality of select signals for selecting the plurality of memory circuits in a test mode, wherein the plurality of memory circuits perform data writing and data reading in accordance with the plurality of select signals;

a multiplexer coupled to the plurality of memory circuits and the processing unit for supplying the processing unit with read data read from one memory circuit which is accessed by the processing unit; and

a comparator coupled to the plurality of memory circuits for comparing plural pieces of read data respectively read from the plurality of memory circuits with one another in the test mode, wherein in the test mode, the processing unit compares data written in the plurality of memory circuits with the read data from the multiplexer to determine whether the write data coincides with the read data.

7. The semiconductor device according to claim 6, wherein the address decoder generates the plurality of select signals based on an address signal for a predetermined one memory circuit and wherein the multiplexer receives the plurality of select signals from the address decoder and supplies data read from the predetermined one memory circuit to the processing unit based on the plurality of select signals in the test mode.

8. The semiconductor device according to claim 6, wherein the address decoder decodes the address signal to generate a decode signal and wherein the multiplexer receives

the decode signal from the address decoder and supplies data read from one of the plurality of memory circuits to the processing unit in accordance with the decode signal.

9. The semiconductor device according to claim 6, wherein the comparator temporarily holds results of comparing the plural pieces of read data with one another.

10. The semiconductor device according to claim 6, wherein the comparator supplies an interruption signal to the processing unit when the plural pieces of read data do not coincide with one another.

11. The semiconductor device according to claim 6, wherein the comparator includes a memory circuit for temporarily holding results of comparing the plural pieces of read data with one another.

12. The semiconductor device according to claim 6, wherein the comparator includes a first memory circuit for temporarily holding the plural pieces of read data.

13. The semiconductor device according to claim 12, wherein the comparator includes a second memory circuit for temporarily holding results of comparing the plural pieces of read data with one another.

14. A system for testing a plurality of memory circuits included in a semiconductor device, comprising:

an address decoder for selecting the plurality of memory circuits and causing the memory circuits to perform a read/write operation;

a comparator for receiving plural pieces of read data

read from the plurality of memory circuits and comparing the plural pieces of read data with one another; and

a processing unit for comparing one of the plural pieces of read data with write data.

15. The system according to claim 14, further comprising a multiplexer for receiving the plural pieces of read data and supplying a specific one of the plural pieces of read data to the processing unit.

16. The system according to claim 14, wherein the comparator includes a memory circuit for temporarily holding results of comparing the plural pieces of read data with one another.

17. The system according to claim 14, wherein the comparator includes a first memory circuit for temporarily holding the plural pieces of read data.

18. The system according to claim 17, wherein the comparator includes a second memory circuit for temporarily holding results of comparing the plural pieces of read data with one another.